# MT7628/7688
# 802.11 b/g/n Wi-Fi APSoC chip EEPROM Content Programming guide

Version: 2.0
Release date: 2014-09-15

# Document Revision History

## EEPROM Changes LOG

| Revision | Date | Author | Change Log |
|---|---|---|---|
| 1.0 | 2014/7/16 | PeterCT Wu | Formal Released |
| 2.0 | 2014/9/15 | PeterCT Wu | 1. Define MAC0: 0x28~0x2D, MAC1: 0x2E ~ 0x33<br>2. Define 0x24[4] : 1x1 downgrade package<br>3. Define 0x24[3:0]: IO setting (for 7628N)<br>4. Re-define 0xF8[7:0] definition (delete bit[7]:valid) and default is 0xA<br>5. Define 0xC6 ~ 0xD6 (Temperature compensation) 00 00 00 1A 22 2A 31 35 - 01 35 39 40 46 4D 7F 7F - 7F<br>6. Define 0xF4=C0 (XTAL calibration)<br>7. Define TSSI offset (AN) 0x57=CA, 0x5D=CA (KN) 0x57=C8, 0x5D=C8<br>8. Remove 0x40 (define on 0x35)<br>9. Rev2_0 |

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# 1 General Description

## 1.1 General Descriptions

The MT7628/7688 EEPROM layout provides configuration for vendor/product ID, MAC Address, SW setting, RF TX power setting.

# 2 MT7628/7688 EEPROM Layout

**Module name: EEPROM Base address: (+0h)**

| Name | Offset | Type | Byte | Reset | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CHIP_ID | 0000 | DC | 1 | 76 | CHIP_ID[15:8] | | | | | | | |
| | | | 0 | 28 | CHIP_ID[7:0] | | | | | | | |
| EEPROM_REV | 0002 | DC | 1 | 02 | REL_REV | | | | | | | |
| | | | 0 | 00 | ENG_REV | | | | | | | |
| WLAN_MAC_B1B0 | 0004 | RW | 1 | 0C | MAC_ADDR_L[15:8] | | | | | | | |
| | | | 0 | 00 | MAC_ADDR_L[7:0] | | | | | | | |
| WLAN_MAC_B3B2 | 0006 | RW | 1 | E1 | MAC_ADDR_M[15:8] | | | | | | | |
| | | | 0 | 43 | MAC_ADDR_M[7:0] | | | | | | | |
| WLAN_MAC_B5B4 | 0008 | RW | 1 | 28 | MAC_ADDR_H[15:8] | | | | | | | |
| | | | 0 | 76 | MAC_ADDR_H[7:0] | | | | | | | |
| MAC0_B1B0 | 0028 | RW | 1 | 0C | MAC0_ADDR_L[15:8] | | | | | | | |
| | | | 0 | 00 | MAC0_ADDR_L[7:0] | | | | | | | |
| MAC0_B3B2 | 002A | RW | 1 | E1 | MAC0_ADDR_M[15:8] | | | | | | | |
| | | | 0 | 43 | MAC0_ADDR_M[7:0] | | | | | | | |
| MAC0_B5B4 | 002C | RW | 1 | 29 | MAC0_ADDR_H[15:8] | | | | | | | |
| | | | 0 | 76 | MAC0_ADDR_H[7:0] | | | | | | | |
| MAC1_B1B0 | 002E | RW | 1 | 0C | MAC1_ADDR_L[15:8] | | | | | | | |
| | | | 0 | 00 | MAC1_ADDR_L[7:0] | | | | | | | |
| MAC1_B3B2 | 0030 | RW | 1 | E1 | MAC1_ADDR_M[15:8] | | | | | | | |
| | | | 0 | 43 | MAC1_ADDR_M[7:0] | | | | | | | |
| MAC1_B5B4 | 0032 | RW | 1 | 2A | MAC1_ADDR_H[15:8] | | | | | | | |
| | | | 0 | 76 | MAC1_ADDR_H[7:0] | | | | | | | |
| NIC_CONFG_0 | 0034 | RW | 1 | 34 | EXT_PA_ANTSEL | | BOARD_TYPE | | | EXT_PA_DRV | EXT_2P4G_PA | EXT_5G_PA |
| | | | 0 | 22 | TX_PATH | | | | RX_PATH | | | |
| NIC_CONFG_1 | 0036 | RW | 1 | 00 | DAC_TEST | | TSSI_COMP | ANT_DIV_CTRL | | | | BW_40M_2P4G |
| | | | 0 | 00 | WPS | | | | WF1_AUX | WF0_AUX | TX_POWER | HW_RADIO |
| COUNTRY_REG | 39 | RW | 0 | 00 | BAND_2P4G | | | | | | | |
| LED_MODE | 3B | RW | 0 | 01 | LED_CTRL | | | | | | | |
| NIC_CONFG_2 | 0042 | RW | 1 | 00 | | | | | TEMP_COMP | XTAL_OPT | | ANT_DIV |
| | | | 0 | 22 | TX_STREAM | | | | RX_STREAM | | | |
| EXT_LNA_GAIN | 44 | RW | 0 | 00 | EXT_LNA_2P4G | | | | | | | |
| RSSI_OFST | 0046 | RW | 1 | 00 | RSSI1_OFST | | | | | | | |
| | | | 0 | 00 | RSSI0_OFST | | | | | | | |
| TX_POWER_DELTA | 50 | RW | 0 | 82 | DELTA_EN | DELTA_IN | DELTA | | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | | C | |
| **TEMP_SEN_CAL** | 55 | **RW** | 0 | Bo | TEMP_COMP_EN | THADC_SLOP | |
| **TX0_PA_TSSI_LSB** | 56 | **RW** | 0 | Co | TX0_PA_TSSI_OFST | | TX0_PA_TSSI_SLOP |
| **TX0_PA_TSSI_MSB** | 57 | **RW** | 0 | CC | TX0_PA_TSSI_OFST | | |
| **TX0_POWER** | 58 | **RW** | 0 | 23 | TX0_TX_PWR | | |
| **TX0_PWR_OFST_L** | 59 | **RW** | 0 | 00 | TX0_TX_PWR_EN | TX0_TX_PWR_INC | TX0_TX_PWR_OFST_L |
| **TX0_PWR_OFST_M** | 5A | **RW** | 0 | 00 | TX0_TX_PWR_EN | TX0_TX_PWR_INC | TX0_TX_PWR_OFST_M |
| **TX0_PWR_OFST_H** | 5B | **RW** | 0 | 00 | TX0_TX_PWR_EN | TX0_TX_PWR_INC | TX0_TX_PWR_OFST_H |
| **TX1_PA_TSSI_LSB** | 5C | **RW** | 0 | 40 | TX1_PA_TSSI_OFST | | TX1_PA_TSSI_SLOP |
| **TX1_PA_TSSI_MSB** | 5D | **RW** | 0 | CC | TX1_PA_TSSI_OFST | | |
| **TX1_POWER** | 5E | **RW** | 0 | 23 | TX1_TX_PWR | | |
| **TX1_PWR_OFST_L** | 5F | **RW** | 0 | 00 | TX1_TX_PWR_EN | TX1_TX_PWR_INC | TX1_TX_PWR_OFST_L |
| **TX1_PWR_OFST_M** | 60 | **RW** | 0 | 00 | TX1_TX_PWR_EN | TX1_TX_PWR_INC | TX1_TX_PWR_OFST_M |
| **TX1_PWR_OFST_H** | 61 | **RW** | 0 | 00 | TX1_TX_PWR_EN | TX1_TX_PWR_INC | TX1_TX_PWR_OFST_H |
| **TX_PWR_CCK_0** | A0 | **RW** | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| **TX_PWR_CCK_1** | A1 | **RW** | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| **TX_PWR_OFDM_0** | A2 | **RW** | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| **TX_PWR_OFDM_1** | A3 | **RW** | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| **TX_PWR_OFDM_2** | A4 | **RW** | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| **TX_PWR_OFDM_3** | A5 | **RW** | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| **TX_PWR_OFDM_4** | A6 | **RW** | 0 | C6 | TX_P | TX_P | TX_PWR_DELTA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | | | WR_COMP_EN | WR_INC | |
| TX_PWR_HT_MCS_0 | A7 | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| TX_PWR_HT_MCS_1 | A8 | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| TX_PWR_HT_MCS_2 | A9 | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| TX_PWR_HT_MCS_3 | AA | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| TX_PWR_HT_MCS_4 | AB | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| TX_PWR_HT_MCS_5 | AC | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| TX_PWR_HT_MCS_6 | AD | RW | 0 | C6 | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA |
| EXT_LNA_RX_GAIN | C0 | RW | 0 | 00 | EXT_LNA | | |
| EXT_LNA_RX_NF | C1 | RW | 0 | 00 | EXT_LNA | | |
| EXT_LNA_RX_P1DB | C2 | RW | 0 | 00 | EXT_LNA | | |
| EXT_LNA_BP_GAIN0 | C3 | RW | 0 | 00 | EXT_LNA | | |
| EXT_LNA_BP_GAIN1 | C4 | RW | 0 | 00 | EXT_LNA | | |
| EXT_LNA_BP_P1DB | C5 | RW | 0 | 00 | EXT_LNA | | |
| STEP_NUM_NEG_7 | C6 | RW | 0 | 00 | STEP_NUM | | |
| STEP_NUM_NEG_6 | C7 | RW | 0 | 00 | STEP_NUM | | |
| STEP_NUM_NEG_5 | C8 | RW | 0 | 00 | STEP_NUM | | |
| STEP_NUM_NEG_4 | C9 | RW | 0 | 1A | STEP_NUM | | |
| STEP_NUM_NEG_3 | CA | RW | 0 | 22 | STEP_NUM | | |
| STEP_NUM_NEG_2 | CB | RW | 0 | 2A | STEP_NUM | | |
| STEP_NUM_NEG_1 | CC | RW | 0 | 31 | STEP_NUM | | |
| STEP_NUM_NEG_0 | CD | RW | 0 | 35 | STEP_NUM | | |
| STEP_NUM_REF | CE | RW | 0 | 01 | STEP_REF | | |
| STEP_NUM_TEMP | CF | RW | 0 | 35 | STEP_TEMP | | |
| STEP_NUM_POS_1 | D0 | RW | 0 | 39 | STEP_NUM | | |
| STEP_NUM_POS_2 | D1 | RW | 0 | 40 | STEP_NUM | | |
| STEP_NUM_POS_3 | D2 | RW | 0 | 46 | STEP_NUM | | |
| STEP_NUM_POS_4 | D3 | RW | 0 | 4D | STEP_NUM | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| STEP_NUM_POS_5 | D4 | RW | 0 | 7F | STEP_NUM | | |
| STEP_NUM_POS_6 | D5 | RW | 0 | 7F | STEP_NUM | | |
| STEP_NUM_POS_7 | D6 | RW | 0 | 7F | STEP_NUM | | |
| XTAL_CAL | F4 | RW | 0 | C0 | XTAL_CAP_VLD | XTAL_CAP | |
| XTAL_TRIM2 | F5 | RW | 0 | 00 | XTAL_TRIM2_EN | XTAL_TRIM2_DEC | XTAL_TRIM2 |
| XTAL_TRIM3 | F6 | RW | 0 | 00 | XTAL_TRIM3_EN | XTAL_TRIM3_DEC | XTAL_TRIM3 |

## 2.1 Chip ID (0x00h)

**0000** **CHIP_ID** **Chip Identifier** **7628**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | CHIP_ID[15:8] | | | | | | | |
| Type | DC | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CHIP_ID[7:0] | | | | | | | |
| Type | DC | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | CHIP_ID | **Chip ID** |

## 2.2 Layout Revision ID (0x02h)

**0002** **EEPROM_REV** **EEPROM Revision** **0200**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | REL_REV | | | | | | | |
| Type | DC | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ENG_REV | | | | | | | |
| Type | DC | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:8 | REL_REV | **Revision for formal release** |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | ENG_REV | **Revision for engineer sample** |

## 2.3 WIFI MAC Address(0x04h)

**0004** **WLAN_MAC_B1B0** **WLAN MAC Address Low Bye** **0C00**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC_ADDR_L[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC_ADDR_L[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC_ADDR_L | **WLAN MAC Address Byte 1/0** |

**0006** **WLAN_MAC_B3B2** **WLAN MAC Address Middle Byte** **E143**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC_ADDR_M[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC_ADDR_M[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC_ADDR_M | **WLAN MAC Address Byte 3/2** |

**0008** **WLAN_MAC_B5B4** **WLAN MAC Address High Byte** **2876**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC_ADDR_H[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC_ADDR_H[7:0] | | | | | | | |
| Type | RW | | | | | | | |

| Reset | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC_ADDR_H | **WLAN MAC Address Byte 5/4** |

## 2.4 WIFI MAC Address(0x28h)

**0028** **MAC0_B1B0** **MAC 0 Address Low Bye** **0C00**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC0_ADDR_L[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC0_ADDR_L[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC0_ADDR_L | **MAC 0 (LAN) Address Byte 1/0** |

**002A** **MAC0_B3B2** **MAC 0 Address Middle Byte** **E143**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC0_ADDR_M[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC0_ADDR_M[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC0_ADDR_M | **MAC 0 (LAN) Address Byte 3/2** |

**002C** **MAC0_B5B4** **MAC 0 Address High Byte** **2976**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC0_ADDR_H[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC0_ADDR_H[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC0_ADDR_H | **MAC 0 (LAN) Address Byte 5/4** |

## 2.5 WIFI MAC Address(0x2Eh)

**002E** **MAC1_B1B0** **MAC 1 Address Low Bye** **0C00**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC1_ADDR_L[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC1_ADDR_L[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC1_ADDR_L | **MAC 1 (WAN) Address Byte 1/0** |

**0030** **MAC1_B3B2** **MAC 1 Address Middle Byte** **E143**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC1_ADDR_M[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC1_ADDR_M[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC1_ADDR_M | **MAC 1 (WAN) Address Byte 3/2** |

**0032** **MAC1_B5B4** **MAC 1 Address High Byte** **2A76**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | MAC1_ADDR_H[15:8] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAC1_ADDR_H[7:0] | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | MAC1_ADDR_H | **MAC 1 (WAN) Address Byte 5/4** |

## 2.6 NIC Configuration 0 (0x34h)

**0034** **NIC_CONFG_0** **NIC Configuration #0** **3422**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_PA_ANTSEL | | BOARD_TYPE | | | EXT_PA_DRV | EXT_2P4G_PA | EXT_5G_PA |
| Type | RW | | RW | | | RW | RW | RW |
| Reset | 0 | 0 | 1 | 1 | | 1 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TX_PATH | | | | RX_PATH | | | |
| Type | RW | | | | RW | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:14 | EXT_PA_ANTSEL | **External PA ANTSEL Table** |
| 13:12 | BOARD_TYPE | **Board Type** |
| 10 | EXT_PA_DRV | **Exteral PA Driving**<br>0: 16mA<br>1: 8 mA |
| 9 | EXT_2P4G_PA | **External 2.4G PA Enable**<br>0: Disable<br>1: Enable |
| 8 | EXT_5G_PA | **External 5G PA Enable**<br>0: Disable<br>1: Enable |
| 7:4 | TX_PATH | **TX Path Setting**<br>These fields are to provide the TX front-end architecture in the system.<br>0: Reserved.<br>1: 1 TX front-end in the system.<br>2: 2 TX front-end in the system.<br>Other: Reserved |
| 3:0 | RX_PATH | **RX Path Setting**<br>These fields are to provide the RX front-end architecture in the system.<br>0: Reserved.<br>1: 1 RX front-end in the system.<br>2: 2 RX front-end in the system.<br>Other: reserved |

## 2.7 NIC Configuration 1 (0x36h)

**0036** **NIC_CONFG_1** **NIC** **0000**

**Configuration #1**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | DAC_TEST | | TSSI_COMP | ANT_DIV_CTRL | | | | BW_40M_2P4G |
| Type | RW | | RW | RW | | | | RW |
| Reset | 0 | | 0 | 0 | 0 | | | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | WPS | | | | WF1_AUX | WF0_AUX | TX_POWER | HW_RADIO |
| Type | RW | | | | RW | RW | RW | RW |
| Reset | 0 | | | | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15 | DAC_TEST | **DAC test bit** |
| 13 | TSSI_COMP | **TSSI power compensation enable**<br>0: disable TSSI power compensation , use per-channel ALC code<br>1: enable TSSI power compensation, TSSI slop offset scheme. |
| 12:11 | ANT_DIV_CTRL | **Antenna Diversity control**<br>00: disable diversity function (default value).<br>01: enable diversity function.<br>10: Fix antenna at main antenna<br>11: Fix antenna at auxiliary antenna |
| 8 | BW_40M_2P4G | **40M BW in 2.4GHz band**<br>0: enable 40MHz bandwidth for 2.4GHz band<br>1: disable 40MHz bandwidth for 2.4GHz band |
| 7 | WPS | **WPS Push Button Configuration control.**<br>0: disable WPS PBC control (default value).<br>1: enable WPS PBC control. |
| 3 | WF1_AUX | **WF1 Aux Rx path selection**<br>0: Use Main path Rx path, board select main rx path as rx data in.<br>1: Use Aux Rx path, need to set, board select aux rx path as rx data in. In this mode, FW also refer 0xC0~0xC5 as external LNA gain setting. |
| 2 | WF0_AUX | **WF0 Aux Rx path selection**<br>0: Use Main path Rx path, board select main rx path as rx data in.<br>1: Use Aux Rx path, need to set, board select aux rx path as rx data in. In this mode, FW also refer 0xC0~0xC5 as external LNA gain setting. |
| 1 | TX_POWER | **TX power temperature compensation scheme enable**<br>This bit will disable/enable temperature compensation scheme. While this bit is enable, it means Tx power TSSI scheme is disable(0x37 bit5 = 0) and using per-channel Tx ALC code scheme.<br>0: disable temperature compensation<br>1: Enable temperature compensation |
| 0 | HW_RADIO | **HW Radio Control**<br>When "hardware radio control" bit is enabled (=1), the driver will read MAC's GPIO[2] status. When GPIO[2] pin is low, the radio is disabled. When GPIO[2] pin is high, the radio is enabled.<br>The Radio ON/OFF is controlled by both software UI and MAC's GPIO[2] pin.<br>0: disable hardware radio control (default value).<br>1: enable hardware radio control. |

## 2.8 Country Region Code for 2.4G band (0x39h)

| 39 | COUNTRY_REG | Country Region 2.4G Band | 00 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | BAND_2P4G | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | BAND_2P4G | **Country Region 2.4G Band**<br>Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value.<br>CountryCode - specify the domain code, can be FFh or one of the followings,<br>0: CH1 - 11<br>1: CH1 - 13<br>2: CH10 - 11<br>3: CH10 - 13<br>4: CH14<br>5: CH1 - 14<br>6: CH3 - 9<br>7: CH5 - 13<br>30: Manual Channel setting (Refer to 0x100~101h for detail)<br>31: CH1 - 14 (CH1 - 11 active scan, CH12 - 14 passive scan)<br>32: CH1 - 13 (CH1 - 11 active scan, CH12 ~ 13 passive scan)<br>33: 802.11b: CH1 to CH14 are active scan. 802.11g/n: CH1 to CH13 are active scan. CH14 is disallowed |

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value.

Notes: If set to read SKU from EEPROM, only available if 2.4G Country Region code registers are programmed.

## 2.9 LED Mode (0x3Bh)

| 3B | LED_MODE | LED Mode Setting | 01 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | LED_CTRL | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | LED_CTRL | **LED Control Modes** |

## 2.10 NIC Configuration 2 (0x42h)

**0042** **NIC_CONFG_2** **NIC Configuration #2** **0022**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | | TEMP_COMP | XTAL_OPT | | ANT_DIV |
| Type | | | | | RW | RW | | RW |
| Reset | | | | | 0 | 0 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TX_STREAM | | | | RX_STREAM | | | |
| Type | RW | | | | RW | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 11 | TEMP_COMP | **25C Temper Compsation Disable**<br>1: disable<br>0: enable |
| 10:9 | XTAL_OPT | **XTAL Option** |
| 8 | ANT_DIV | **HW ANT Diversity**<br>0: Disable<br>1: Enable |
| 7:4 | TX_STREAM | **TX Stream**<br>1: 1 stream<br>2: 2 stream |
| 3:0 | RX_STREAM | **RX Stream**<br>1: 1 stream<br>2: 2 stream |

## 2.11 RSSI Offset for 2.4G band (0x46h)

**0046** **RSSI_OFST** **2.4G RSSI Offset** **0000**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | RSSI1_OFST | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RSSI0_OFST | | | | | | | |
| Type | RW | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|

| Bit(s) | Name | Description |
|---|---|---|
| 15:8 | RSSI1_OFST | **2.4 G RSSI 1 Offset** |
| 7:0 | RSSI0_OFST | **2.4 G RSSI 0 Offset** |

## 2.12 20M/40M BW Power Delta for 2.4G band (0x50h)

| 50 | TX_POWER_DELTA | 20/40 BW TX Power Delta for 2.4G | 82 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | DELTA_EN | DELTA_INC | DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | DELTA_EN | **Power Delta Enable Bit**<br>0: Disable<br>1: Enable |
| 6 | DELTA_INC | **Power Delta Increase**<br>0: Decrease<br>1: Increase |
| 5:0 | DELTA | **Delta Value**<br>000001: 0.5dBm<br>000010: 1dBm<br>000011: 1.5dBm<br>000100: 2dBm<br>000101: 2.5dBm<br>000110: 3dBm<br>000111: 3.5dBm<br>001000: 4dBm |

**Example:**

The default calibrated TX power as followings with the TX power delta configuration is not enable.

- 40M BW TX power= 14dBm and 20M BW TX power = 14dBm

If want keep 20M BW TX power in 14dBm and reduce 40M BW TX power to 10dBm (delta=4dBm), set 50h = 88h (1000 1000).

## 2.13 Temp. Sensor Calibration (0x55h)

| 55 | TEMP_SEN_CAL | Temperature | Bo |
|---|---|---|---|

**Sensor Calibration**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TEMP_COMP_EN | THADC_SLOP | | | | | | |
| Type | RW | RW | | | | | | |
| Reset | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TEMP_COMP_EN | **Temperature Compensation Enable**<br>[note] Calibration-free Field<br>0: Disable<br>1: Enable |
| 6:0 | THADC_SLOP | **THADC cal read out value**<br>This is THADC read out value, this value should follow the temp. formulation to get the temperature.<br>[note] Calibration-free Field |

## 2.14 2.4G Tx0 Power Slope /offset (0x56h~0x57h)

**56** **TX0_PA_TSSI_LSB** **TX0 PA TSSI slop and Offset** **Co**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX0_PA_TSSI_OFST | | | | TX0_PA_TSSI_SLOP | | | |
| Type | RW | | | | RW | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:4 | TX0_PA_TSSI_OFST | **TX0 2.4G TX PA TSSI_Offset[3:0]**<br>[note] Calibration-free Field |
| 3:0 | TX0_PA_TSSI_SLOP | **TX0 2.4G TX PA TSSI Slop**<br>[note] Calibration-free Field |

**57** **TX0_PA_TSSI_MSB** **TX0 PA TSSI Offset MSB** **CC**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX0_PA_TSSI_OFST | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | TX0_PA_TSSI_OFST | **TX0 2.4G TX PA TSSI_Offset[11:4]** |

| Bit(s) | Name | Description |
|---|---|---|
| | | [note] Calibration-free Field<br>0xCA: 7628 A/N<br>0xC8: 7628K |

Driver compares current TSSI value with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value. This function is controlled by 'external TX ALC' bit (NIC configuration1 bit1) or 'internal TX ALC ' bit (NIC configuration1 bit13).

## 2.15 2.4G Tx0 Target Power (0x58h)

**58** **TX0_POWER** **TX0 TX Power** **23**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX0_TX_PWR | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | TX0_TX_PWR | **TX0 2.4G TX power (54Mbps, dBm)** |

## 2.16 2.4G Tx0 Power Low/Middle/High Channel (0x59h ~ 0x5Bh)

**59** **TX0_PWR_OFST_L** **TX0 TX Power Offset Low** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX0_TX_PWR_EN | TX0_TX_PWR_INC | TX0_TX_PWR_OFST_L | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX0_TX_PWR_EN | **TX0 2.4G TX power offset Enable**<br>0: Disable<br>1: Enable |
| 6 | TX0_TX_PWR_INC | **TX0 2.4G TX power offset Increase**<br>0: Decrease<br>1: Increase |
| 5:0 | TX0_TX_PWR_OFST_L | **TX0 2.4G TX power offset low(CH1~5)(delta,dB)** |

**5A** **TX0_PWR_OFST_M** **TX0 TX Power Offset Middle** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX0_TX_PWR_EN | TX0_TX_PWR_INC | TX0_TX_PWR_OFST_M | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX0_TX_PWR_EN | **TX0 2.4G TX power offset Enable**<br>0: Disable<br>1: Enable |
| 6 | TX0_TX_PWR_INC | **TX0 2.4G TX power offset Increase**<br>0: Decrease<br>1: Increase |
| 5:0 | TX0_TX_PWR_OFST_M | **TX0 2.4G TX power offset middle(CH6~10)(delta,dB)** |

**5B** **TX0_PWR_OFST_H** **TX0 TX Power Offset High** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX0_TX_PWR_EN | TX0_TX_PWR_INC | TX0_TX_PWR_OFST_H | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX0_TX_PWR_EN | **TX0 2.4G TX power offset Enable**<br>0: Disable<br>1: Enable |
| 6 | TX0_TX_PWR_INC | **TX0 2.4G TX power offset Increase**<br>0: Decrease<br>1: Increase |
| 5:0 | TX0_TX_PWR_OFST_H | **TX0 2.4G TX power offset high(CH11~14)(delta,dB)** |

0x59~0x5B are used as channel TX power compensation in customer production line.
Customers could set different TX power compensation value according to different PCB design to reach flatter power responds.
For example
If customers found PCB had 1.5dB higher power variation in low channels and 1.5dB lower power variation in high channels.
Customer could use channel compensation offset to get flatter performance like setting as below.

| Offset | Description | Example |
|---|---|---|
| 0x59 | TX0 2.4G Tx power offset low (CH1~5)(delta,dB) | 0x83=> means SW will decrease 3 step(around -1.5dB) corresponding to TX0 2.4G TX power setting. |
| 0x5A | TX0 2.4G Tx power offset middle (CH6~10)(delta,dB) | 0x80=> means SW will decrease 0 step(around 0dB) corresponding to TX0 2.4G TX power setting. |
| 0x5B | TX0 2.4G Tx power offset high (CH11~14)(delta,dB) | 0xC3=> means SW will increase 3 step(around +1.5dB) corresponding to TX0 2.4G TX power setting. |

## 2.17 2.4G Tx1 Power Slope /offset (0x5Ch~0x5Dh)

**5C** **TX1_PA_TSSI_LSB** **TX1 PA TSSI slop and Offset** **40**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX1_PA_TSSI_OFST | | | | TX1_PA_TSSI_SLOP | | | |
| Type | RW | | | | RW | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:4 | TX1_PA_TSSI_OFST | **TX1 2.4G TX PA TSSI Offset[3:0]**<br>[note] Calibration-free Field |
| 3:0 | TX1_PA_TSSI_SLOP | **TX1 2.4G TX PA TSSI Slop**<br>[note] Calibration-free Field |

**5D** **TX1_PA_TSSI_MSB** **TX1 PA TSSI Offset MSB** **CC**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX1_PA_TSSI_OFST | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | TX1_PA_TSSI_OFST | **TX1 2.4G TX PA TSSI Offset[11:4]**<br>[note] Calibration-free Field |

## 2.18 2.4G Tx1 Target Power (0x5Eh)

**5E** **TX1_POWER** **TX1 TX** **23**

**Power**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX1_TX_PWR | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | TX1_TX_PWR | **TX1 2.4G TX power (54Mbps, dBm)** |

## 2.19 2.4G Tx1 Power Offset Low/Middle/High Channel(0x5Fh~0x61h)

**5F** **TX1_PWR_OFST_L** **TX1 TX Power Offset Low** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX1_TX_PWR_EN | TX1_TX_PWR_INC | TX1_TX_PWR_OFST_L | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX1_TX_PWR_EN | **TX1 2.4G TX power offset Enable**<br>0: Disable<br>1: Enable |
| 6 | TX1_TX_PWR_INC | **TX1 2.4G TX power offset Increase**<br>0: Decrease<br>1: Increase |
| 5:0 | TX1_TX_PWR_OFST_L | **TX1 2.4G TX power offset low(CH1~5)(delta,dB)** |

**60** **TX1_PWR_OFST_M** **TX1 TX Power Offset Middle** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX1_TX_PWR_EN | TX1_TX_PWR_INC | TX1_TX_PWR_OFST_M | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX1_TX_PWR_EN | **TX1 2.4G TX power offset Enable**<br>0: Disable<br>1: Enable |
| 6 | TX1_TX_PWR_INC | **TX1 2.4G TX power offset Increase**<br>0: Decrease<br>1: Increase |

| Bit(s) | Name | Description |
|---|---|---|
| 5:0 | TX1_TX_PWR_OFST_M | **TX1 2.4G TX power offset middle(CH6~10)(delta,dB)** |

**61** **TX1_PWR_OFST_H** **TX1 TX Power Offset High** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX1_TX_PWR_EN | TX1_TX_PWR_INC | TX1_TX_PWR_OFST_H | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX1_TX_PWR_EN | **TX1 2.4G TX power offset Enable**<br>0: Disable<br>1: Enable |
| 6 | TX1_TX_PWR_INC | **TX1 2.4G TX power offset Increase**<br>0: Decrease<br>1: Increase |
| 5:0 | TX1_TX_PWR_OFST_H | **TX1 2.4G TX power offset high(CH11~14)(delta,dB)** |

## 2.20 2.4G Tx rate power configuration (0xA0h~0xBFh)

**A0** **TX_PWR_CCK_0** **2.4GHz TX Power for CCK 1M/2M** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A1** **TX_PWR_CCK_1** **2.4GHz** **C6**

**TX Power for CCK 5.5M/11M**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A2** **TX_PWR_OFDM_0** **2.4GHz TX Power for OFDM 6M/9M** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A3** **TX_PWR_OFDM_1** **2.4GHz TX Power for OFDM 12M/18M** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A4** **TX_PWR_OFDM_2** **2.4GHz TX Power for OFDM 24M/36M** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A5** **TX_PWR_OFDM_3** **2.4GHz TX Power for OFDM 48M** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A6** **TX_PWR_OFDM_4** **2.4GHz TX Power for OFDM 54M** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A7** **TX_PWR_HT_MCS_0** **2.4GHz TX Power for HT MCS=0/8** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A8** **TX_PWR_HT_MCS_1** **2.4GHz TX Power for HT MCS=32** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**A9** **TX_PWR_HT_MCS_2** **2.4GHz TX Power for HT MCS=1,2/ 9,10** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**AA** **TX_PWR_HT_MCS_3** **2.4GHz TX Power for HT MCS=3,4/ 11,12** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**AB** **TX_PWR_HT_MCS_4** **2.4GHz TX Power for HT MCS=5/13** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**AC** **TX_PWR_HT_MCS_5** **2.4GHz TX Power for HT MCS=6/14** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_COMP_EN | TX_PWR_INC | TX_PWR_DELTA | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

**AD** **TX_PWR_HT_MCS_6** **2.4GHz TX Power for HT MCS=7/15** **C6**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | TX_PWR_C | TX_PWR_I | TX_PWR_DELTA | | | | | |

| | OMP_EN | NC | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Type | RW | RW | RW | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | TX_PWR_COMP_EN | **Power Compesation Enable**<br>0: Disable<br>1: Enable |
| 6 | TX_PWR_INC | **Increase TX Power with the Delta Value**<br>0: Decrease<br>1: Increase |
| 5:0 | TX_PWR_DELTA | **TX Power Delta (delta, dB)** |

Default value=0x00, 6bit signed 2's complement value. (1 step=0.5dBm)
0xA0~0xBE are used as TX rate power configuration in customer production line.
Customers could set different TX rate power according to different RF power requirement.

Example:

If the table content is :

| Offset | Ex. Value | Description | Example description |
|---|---|---|---|
| A0h | C3 | 2G TX power for CCK 1M/2M | 0xC3=><br>2G 1~11M & 6~18M will have 1.5dB higher power than 54M.<br>0x00=><br>2G 24~54M will have equal power with 54M. |
| A1h | C3 | 2G TX power for CCK 5.5M/11M | |
| A2h | C3 | 2G TX power for OFDM 6M/9M | |
| A3h | C3 | 2G TX power for OFDM 12M/18M | |
| A4h | 0 | 2G TX power for OFDM 24M/36M | |
| A5h | 0 | 2G TX power for OFDM 48M | |
| A6h | 0 | 2G TX power for OFDM 54M | |
| A7h | C2 | 2G TX power for HT/VHT MCS=0/8 | 0xC2 =><br>2G HT MCS0~3 &MCS8~11 will have 1dB higher power than 54M.<br>0x82 =><br>2G HT MCS4~7 &MCS12~15 will have 1dB lower power than 54M.<br><br>0xC2=><br>5G HT MCS0~3 &MCS8~11 will have 1dB higher power than 54M.<br>5G VHT MCS0~3 will have 1dB higher power than 54M.<br>0x82=><br>5G HT MCS4~7 &MCS12~15 will have 1dB lower power than 54M.<br>5G VHT MCS4~7 will have 1dB lower power than 54M. |
| A8h | C2 | 2G TX power for HT/VHT MCS=32 | |
| A9h | 82 | 2G TX power for HT/VHT MCS=1,2/9,10 | |
| AAh | 82 | 2G TX power for HT/VHT MCS=3,4/11,12 | |
| ABh | C2 | 2G TX power for HT MCS=5/13 | |
| ACh | C2 | 2G TX power for HT MCS=6/14 | |
| ADh | 82 | 2G TX power for HT MCS=7/15 | |

## 2.21 External LNA (0xC0h)

| Co | EXT_LNA_RX_GAIN | External LNA RX | oo |
|---|---|---|---|

**GAIN**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_LNA | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | EXT_LNA | **External LNA** |

**C1** **EXT_LNA_RX_NF** **External LNA RX NF** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_LNA | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | EXT_LNA | **External LNA** |

**C2** **EXT_LNA_RX_P1DB** **External LNA RX P1 DB** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_LNA | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | EXT_LNA | **External LNA** |

**C3** **EXT_LNA_BP_GAIN0** **External LNA BYPASS RX GAIN 0** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_LNA | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | EXT_LNA | **External LNA** |

| C4 | EXT_LNA_BP_GAIN1 | External LNA BYPASS RX GAIN 1 | 00 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | EXT_LNA | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | EXT_LNA | External LNA |

***CODA_REG_EXT_LNA_BP_P2DB***

## 2.22 2.4GHz Step Number (0xC6h)

| C6 | STEP_NUM_NEG_7 | Step Number for -7 | 00 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | Step Number for -7 |

| C7 | STEP_NUM_NEG_6 | Step Number for -6 | 00 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | Step Number for -6 |

| C8 | STEP_NUM_NEG_5 | Step Number for -5 | 00 |
|---|---|---|---|

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |

| Type | RW | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for -5** |

**C9** **STEP_NUM_NEG_4** **Step Number for -4** **1A**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for -4** |

**CA** **STEP_NUM_NEG_3** **Step Number for -3** **22**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for -3** |

**CB** **STEP_NUM_NEG_2** **Step Number for -2** **2A**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for -2** |

**CC** **STEP_NUM_NEG_1** **Step Number for -1** **31**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |

| Type | RW | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Reset | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for -1** |

**CD** **STEP_NUM_NEG_0** **Step Number for -0** **35**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for -0** |

**CE** **STEP_NUM_REF** **2.4GHz Reference Step** **01**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_REF | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_REF | **2.4GHz Reference Step** |

**CF** **STEP_NUM_TEMP** **2.4GHz Reference Temperature** **35**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_TEMP | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_TEMP | **2.4GHz Reference Temperature** |

**D0** **STEP_NUM_POS_1** **Step Number for +1** **39**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +1** |

**D1** **STEP_NUM_POS_2** **Step Number for +2** **40**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +2** |

**D2** **STEP_NUM_POS_3** **Step Number for +3** **46**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +3** |

**D3** **STEP_NUM_POS_4** **Step Number for +4** **4D**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +4** |

**D4** **STEP_NUM_POS_5** **Step Number for +5** **7F**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +5** |

**D5** **STEP_NUM_POS_6** **Step Number for +6** **7F**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +6** |

**D6** **STEP_NUM_POS_7** **Step Number for +7** **7F**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | STEP_NUM | | | | | | | |
| Type | RW | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 7:0 | STEP_NUM | **Step Number for +7** |

## 2.23 Frequency offset (0xF4h ~ 0xF6h)

**F4** **XTAL_CAL** **Frequency Offet (XTAL Calibration)** **Co**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | XTAL_CAP_VLD | XTAL_CAP | | | | | | |
| Type | RW | RW | | | | | | |
| Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|

| Bit(s) | Name | Description |
|---|---|---|
| 7 | XTAL_CAP_VLD | **XTAL Cpa. Code Valid**<br>[note] Calibration-free Field |
| 6:0 | XTAL_CAP | **XTAL Cap. Code**<br>[note] Calibration-free Field |

**F5** **XTAL_TRIM2** **XTAL Trim 2 Compena ton (on RFB)** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | XTAL_TRIM2_EN | XTAL_TRIM2_DEC | XTAL_TRIM2 | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | XTAL_TRIM2_EN | **XTAL Trim 2 Enable**<br>0: Disable<br>1: Enable |
| 6 | XTAL_TRIM2_DEC | **XTAL Trim 2 Decrease**<br>0: Increase<br>1: Decrease |
| 5:0 | XTAL_TRIM2 | **XTAL Trim 2 Value** |

**F6** **XTAL_TRIM3** **XTAL Trim 3 Compena ton** **00**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Name | XTAL_TRIM3_EN | XTAL_TRIM3_DEC | XTAL_TRIM3 | | | | | |
| Type | RW | RW | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | XTAL_TRIM3_EN | **XTAL Trim 3 Enable**<br>0: Disable<br>1: Enable |
| 6 | XTAL_TRIM3_DEC | **XTAL Trim 3 Decrease**<br>0: Increase<br>1: Decrease |
| 5:0 | XTAL_TRIM3 | **XTAL Trim 3 Value** |

0xF4 is used for MTK FT test only for crystal calibration-free feature .

MTK wafer manufactory used 0xF4, bit 0~6, to store frequency offset value which is measured under MTK FT environment. Each IC has each corresponding frequency offset .
Bit 7 of 0xF4 is used to enable to apply crystal code vale. “1” means enable and “0” means disablle. While Bit7 is 0 (disable), it means rom code will not use crystal value of 0xF4 but use crystal code default value in rom code. Default is “1” (enable).
0xF5/0xF6 is used for crystal re-calibration purpose in customer production line
If customers want to re-do frequency trimming in customer production line, please use 0xF5/F6 as second /third frequency offset. Rom/Firmware code will check 0xF5/0xF6 Bit7 to decide the crystal trim code need to be compensated or not. Here is the formula :

**If (0xF4[7] == 1 && 0xF5[7] == 1 && 0xF6[7] == 1)**
**Final xtal trim code = 0xF4[6:0] +/- 0xF5[5:0] +/- 0xF6[5:0];**
**// the increase/descrease(+/-) depends on 0xF5/F6[6]’s value**
**Else if( (0xF4[7] == 1 && 0xF5[7] == 1 )**
**Final xtal trim code = 0xF4[6:0] +/- 0xF5[5:0];**
**Else if( (0xF4[7] == 1)**
**Final xtal trim code = 0xF4[6:0];**
**Else**
**Use rom code default vale.**

## 2.24 Reserved for Customer (0x140h~0x1EFh)